WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a single crystalline underlying layer formed in part of a substrate;

an insulating layer formed in another part of the substrate;

a semiconductor layer epitaxially grown above the underlying layer and having a composition represented by $Si_{1-x1-y1}Ge_{x1}C_{y1}$ (where $0<x1<1$, $0\leqq y1<1$);

a buffer layer epitaxially grown between the underlying layer and the semiconductor layer and having a composition represented by $Si_{1-x2-y2}Ge_{x2}C_{y2}$ (where $0\leqq x2<1$, $0\leqq y2<1$, $1-x2-y2>1-x1-y1$); and

a polycrystalline semiconductor layer formed on the insulating layer and including a semiconductor having substantially the same composition as the buffer layer and a semiconductor having substantially the same composition as the semiconductor layer.

2. The semiconductor device of claim 1, wherein the single crystalline underlying layer is a silicon layer.

3. The semiconductor device of claim 2, wherein the semiconductor layer is an SiGe layer or an SiGeC layer,

wherein the buffer layer is a silicon layer and

wherein the polycrystalline semiconductor layer contains at least SiGe.

4. The semiconductor device of claim 3, wherein the underlying layer is a collector layer,

wherein the semiconductor layer has at least part serving as a base layer and

wherein the polycrystalline semiconductor layer serves as at least part of a base

lead-electrode,

the semiconductor device functioning as a heterojunction bipolar transistor.

5. The semiconductor device of claim 4, wherein the polycrystalline semiconductor layer serves as at least part of a gate electrode of an MIS transistor,

the semiconductor device functioning as a BiCMOS device.

6. The semiconductor device of claim 1, wherein the buffer layer has a thickness of not less than 2 nm nor more than 20 nm.

7. A method for fabricating a semiconductor device, comprising the steps of:

(a) pre-cleaning a substrate including a single crystalline underlying layer having a composition represented by $Si_{1-x3-y3}Ge_{x3}C_{y3}$ (where $0 \leqq x3 < 1$, $0 \leqq y3 < 1$) and an insulating layer;

(b) forming, after the step (a), a buffer layer having a composition represented by $Si_{1-x2-y2}Ge_{x2}C_{y2}$ (where $0 \leqq x2 < 1$, $0 \leqq y2 < 1$) on the underlying layer while depositing a first polycrystalline semiconductor layer having substantially the same composition as the buffer layer on the insulating layer; and

(c) forming, after the step (b), a semiconductor layer having a composition represented by $Si_{1-x1-y1}Ge_{x1}C_{y1}$ (where $0 < x1 < 1$, $0 \leqq y1 < 1$) on the buffer layer while depositing over the insulating layer a second polycrystalline semiconductor layer having substantially the same composition as the semiconductor layer so that the second polycrystalline semiconductor layer covers the first polycrystalline semiconductor layer,

wherein a relation represented by the inequality of $1-x2-y2 > 1-x1-y1$ holds between both the compositions of the semiconductor layer and the buffer layer.

8. The method of claim 7, wherein in the step (b), the first polycrystalline semiconductor is formed as substantially a continuous film.

9. The method of claim 7, wherein the temperature of the substrate is lower when the step (b) is performed than that when the step (c) is performed.

10. The fabrication method of claim 7, wherein the difference between the substrate temperatures in the steps (b) and (c) is within the range from 10 ℃ to 100 ℃.

11. The fabrication method of claim 7, wherein in the step (a), the substrate is held at a high temperature and then the substrate temperature is reduced to a level where the step (b) is performed and

wherein nuclei for epitaxial growth of the first or second polycrystalline semiconductor layer to be performed in the step (c) are formed on the insulating layer at a time point during the temperature reduction in the step (a).

12. The fabrication method of claim 7, wherein the semiconductor layer is an SiGe layer or an SiGeC layer and

wherein the buffer layer is a silicon layer.

13. The fabrication method of claim 7, wherein the underlying layer is a collector layer,

wherein the semiconductor layer has at least part serving as a base layer and

wherein the first and second polycrystalline semiconductor layers serve as at least

parts of a base lead-electrode,

the semiconductor device functioning as a heterojunction bipolar transistor.

14. The fabrication method of claim 13, wherein the first and second polycrystalline layers serve at least parts of an MIS transistor,

the semiconductor device functioning as a BiCMOS device.

15. The fabrication method of claim 7, wherein the steps (b) and (c) are performed under ultra-high vacuum.

16. The fabrication method of claim 7, wherein the temperature of the substrate is in the range from 400 ℃ to 650 ℃ when the steps (b) and (c) are performed.